What is claimed is:

1. A thin film transistor substrate, comprising:

a plurality of gate lines formed on a substrate;

a plurality of data lines insulated from and intersecting said gate lines, said data lines and intersecting gate lines defining a plurality of cells, at least one cell including,

a pixel electrode,

a thin film transistor connected to one of the data lines and one of the gate lines defining the cell,

a storage capacitor, and

a metallic pattern forming a drain electrode of the thin film transistor and a storage electrode of the storage capacitor, and being electrically connected to the pixel electrode.

2. The substrate of claim 1, wherein the metallic pattern is spaced a predetermined distance from the data line connected to the thin film transistor.

3. The substrate of claim 2, further comprising:

a protective layer disposed between the pixel electrode and the metallic pattern, the metallic pattern being overlapped with a portion of a periphery of the pixel electrode.

4. The substrate of claim 1, further comprising:

a protective layer disposed between the pixel electrode and the metallic pattern, the metallic pattern being overlapped with a portion of a periphery of the pixel electrode.

5. The substrate of claim 4, wherein

the metallic pattern has an annular shape, and

an entire periphery of the pixel electrode overlaps the

metallic pattern.

6. The substrate of claim 5, wherein the metallic pattern is spaced a predetermined distance from the data line connected to the thin film transistor.

7. The substrate of claim 1, further comprising:

a protective layer disposed between the pixel electrode and the metallic pattern, the pixel electrode being connected to a source electrode part of the metallic pattern via a first contact hole in the protective layer.

8. The substrate of claim 7, wherein the protective layer does not include a contact hole over a drain electrode part of the metallic pattern.

9. The substrate of claim 8, wherein the drain electrode part has a smaller area than if the drain electrode part was electrically connected to the pixel electrode via a contact hole in the protective layer over the drain electrode part.

10. The substrate of claim 8, wherein the pixel electrode has a larger aspect ratio than if the drain electrode part was electrically connected to the pixel electrode via a contact hole in the protective layer over the drain electrode part.

11. The substrate of claim 8, wherein

the metallic pattern is spaced a predetermined distance from the data line connected to the thin film transistor; and

a portion of a periphery of the pixel electrode overlaps the metallic pattern.

12. The substrate of claim 8, wherein

the metallic pattern has an annular shape and is spaced a predetermined distance from the data line connected to the

thin film transistor; and

an entire periphery of the pixel electrode overlaps the metallic pattern.

13. The substrate of claim 7, wherein

the pixel electrode is connected to a drain electrode part of the metallic pattern via a second contact hole in the protective layer.

14. The substrate of claim 13, wherein

the metallic pattern is spaced a predetermined distance from the data line connected to the thin film transistor; and

a portion of a periphery of the pixel electrode overlaps the metallic pattern.

15. The substrate of claim 13, wherein

the metallic pattern has an annular shape and is spaced a predetermined distance from the data line connected to the thin film transistor; and

an entire periphery of the pixel electrode overlaps the metallic pattern.

16. The substrate of claim 1, further comprising:

a protective layer disposed between the pixel electrode and the metallic pattern, and wherein

the pixel electrode is connected to a drain electrode part of the metallic pattern via a contact hole in the protective layer.

17. The substrate of claim 16, wherein the protective layer does not include a contact hole over a source electrode part of the metallic pattern.

18. The substrate of claim 17, wherein the pixel electrode overlaps a gate line, defining the cell but not

connected to the thin film transistor, less than if the protective layer included a contact hole over a storage electrode part of the metallic pattern.

19. The substrate of claim 17, wherein

the metallic pattern is spaced a predetermined distance from the data line connected to the thin film transistor; and

a portion of a periphery of the pixel electrode overlaps the metallic pattern.

20. The substrate of claim 16, wherein

the metallic pattern has an annular shape and is spaced a predetermined distance from the data line connected to the thin film transistor; and

an entire periphery of the pixel electrode overlaps the metallic pattern.

21. A thin film transistor substrate, comprising:

a plurality of gate lines formed on a substrate;

a plurality of data lines insulated from and intersecting said gate lines, said data lines and intersecting gate lines defining a plurality of cells, at least one cell including,

a pixel electrode,

a thin film transistor selectively electrically connecting one of the data lines to the pixel electrode, and including a source electrode connected to the one of the data lines, a gate electrode connected to one of the gate lines, and a drain electrode, and

a storage capacitor having a storage electrode electrically connected to the drain electrode and the pixel electrode.

22. The substrate of claim 21, further comprising:

a metallic pattern connecting the storage electrode and the drain electrode.

23. A method of manufacturing a thin film transistor substrate, comprising:

forming a plurality gate lines with gate electrodes extending therefrom on a transparent substrate;

forming a gate insulating layer over the substrate;

forming a plurality of data lines intersecting with the gate lines over the substrate, the data lines including source electrodes extending therefrom;

forming a metallic pattern having a drain electrode part and a source electrode part, the source electrode part formed overlapping with one of the gate lines;

forming a semiconductor layer over at least a portion of one of the gate electrodes, at least a portion of one of the source electrodes, and at least a portion of the drain electrode part;

forming a protective film over the substrate, the protective film including a contact hole exposing a portion of the metallic pattern; and

forming a pixel electrode over the protective film and in electrical contact with the metallic pattern via the contact hole.

24. The method of claim 23, wherein the forming a plurality of data lines step and the forming a metallic pattern step are performed simultaneously by forming a conductive layer over the substrate and patterning the conductive layer to form the data lines and the metallic pattern such that the metallic pattern is spaced a predetermined distance from one of the data lines.

25. The method of claim 23, wherein the forming a pixel electrode step forms the pixel electrode such that a portion of a periphery of the pixel electrode overlaps the metallic pattern.

26. The method of claim 23, wherein the forming a pixel electrode step forms the pixel electrode such that an entire periphery of the pixel electrode overlaps the metallic pattern.

27. The method of claim 23, wherein the forming a protective layer step forms the protective layer with a first contact hole exposing the source electrode part of the metallic pattern.

28. The method of claim 27, wherein the forming a protective layer step does not form the protective layer with a contact hole exposing the drain electrode part of the metallic pattern.

29. The method of claim 27, wherein the forming a protective layer step forms the protective layer with a second contact hole exposing the drain electrode part of the metallic pattern.

30. The method of claim 23, wherein the forming a protective layer step forms the protective layer with a contact hole exposing the drain electrode part of the metallic pattern.

31. The method of claim 30, wherein the forming a protective layer step does not form the protective layer with a contact hole exposing the source electrode part of the metallic pattern.